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Question Paper Code : 52920

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2019.

Sixth/Seventh/Eighth Semester

Electronics and Communication Engineering

EC 6601 — VLSI DESIGN

(Common to Electrical and Electronics Engineering, Biomedical Engineering, Electronics and Instrumentation Engineering, Medical Electronics, Robotics and Automation Engineering)

(Regulation 2013)

(Also Common to PTEC 6601 — VLSI Design for B.E. Part-Time – Seventh Semester – Electronics and Communication Engineering – Regulation 2014)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Define threshold voltage of MOSFET.

2. By what factor, gate capacitance must be scaled if constant electric field scaling is employed?

3. State the various types of power dissipation.

4. Draw a 2-input XOR using nMOS pass transistor logic.

5. Define clock skew.

6. Draw a 1-transistor Dynamic RAM cell.

7. Define kill term, propagate and generate term in a carry look ahead adder.

8. State radix-2 booth encoding table.

9. Differentiate full custom and semi-custom design.

10. State the three important blocks in FPGA architecture.

PART B — (5 × 13 = 65 marks)

11. (a) (i) Derive an expression for I_{ds} of nMOS in linear and saturated region. (6)

(ii) Draw a CMOS inverter. Analyze the switching characteristics during rise time when V_{in} changes from high to low. (7)

Or

(b) (i) Draw the stick diagram of CMOS inverter. (7)

(ii) State the minimum width and minimum spacing lambda based design rules to draw the layout. (6)

12. (a) (i) Derive an expression for dynamic power dissipation. (7)

(ii) Realize the following function $Y = (A + BC)D + E$ using static CMOS logic. (6)

Or

(b) Let A, B, C and D be the inputs of a data selector and S0 and S1 be the select lines. Realize a 4:1 data selector using (i) nMOS pass transistor and (ii) transmission gate approach. Compare the hardware complexity. (13)

13. (a) Design a D-latch using Transmission gate. Using which realize a two phase non-overlapping master-slave negative edge triggered D-Flip-flop. (13)

Or

(b) Elucidate in detail low power SRAM circuit. (13)

14. (a) Derive the necessary expressions of a 4-bit carry look ahead adder and realize the carry out expressions using Dynamic CMOS logic. (13)

Or

(b) Design a 4-bit unsigned array multiplier and analyze its hardware complexity. (13)

15. (a) Elucidate in detail the basic FPGA architecture. (13)

Or

(b) Describe FPGA interconnect routing resources with neat diagram. (13)

PART C — (1 × 15 = 15 marks)

16. (a) Realize a 2-input XOR using static CMOS, transmission gate and dynamic CMOS logic. Analyze the hardware complexity. (15)

Or

(b) Apply radix-2 booth encoding to realize a 4-bit signed multiplier for (–10)*(–11). (15)

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